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Effect of fabrication process on hysteresisy of carbon nanotube FETs

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1. INTRODUTION

Carbon nanotube field-effect transistors (CNTFETs) have great advantages over the conventional Si MOS FETs because of their high transconductance and large current driving capability. However, CNTFETs exhibit a large hysteresis in the I_D-V_{GS} characteristics. W. Kim *et al*. have reported that the water molecules on the device surface are the origin of the large hysteresis, which can be suppressed by surface passivation using PMMA [1]. In our experiments, however, the reproducibility was quite poor. In this study, we have statistically studied the hysteresis and the passivation process. The reproducibility of the passivation has been improved by introducing cleaning process before the PMMA passivation.

2. EXPERIMENTS

Figure 1 shows a schematic device structure of the fabricated nanotube FETs [2]. The SWNTs were grown directly on the Si wafer by alcohol catalytic chemical vapor deposition [3]. The present passivation process consists of two steps; a surface coating with PMMA (~2 μm) followed by baking at 180°C for 24 h, and a subsequent SiO_2 (100 nm) cover layer deposition on the PMMA. This cover layer was introduced to secure long-term stability of the passivation. Figure 2 shows the I_D as a function of the V_{GS} of the SiO_2/PMMA-passivated device. Here, the V_{DS} was -0.1 V. This device exhibited negligible hysteresis in the ambient atmosphere. The hysteresis has been suppressed at least for a month. However, the effect of the passivation on the hysteresis depends on devices. In the present case, the passivation was effective only for one device, and did not work for most devices as shown in the histogram of Fig. 3(a).

We have found that the poor reproducibility is related to the device fabrication process, as it will be discussed below. Figure 4(a) shows the variation of hysteresis by baking in vacuum (200°C, 1×10^{-3} Pa) for two batches, with and without the process to form the source and drain electrodes. In the latter case, the catalysts were used as the source and drain electrodes. The hysteresis decreased with baking time for both batches. This is because of the desorption of water molecules near the nanotube. Figure 4(b) is a comparison of the hysreresis between two batches after baking for 96 h. It should be noted that the hysteresis voltage width and the dispersion of the batch without the contact formation process is much smaller than those of the batch with the process. This shows that the hysteresis is related to the contact formation process. The most plausible factor impeding the decrease in the hysteresis is the scum of the photoresist.

In order to remove the scum of the photoresist, we introduced the cleaning process using H_2SO_4:H_2O_2 (4:1) before the SiO_2/PMMA passivation process. Figure 3(b) shows histogram of the hysteresis voltage width of the devices with the cleaning process. In this case, the hysteresis was reduced for most devices by the passivation. The long-term stability was also confirmed.

3. SUMMARY

We have shown that the hysteresis of nanotube FETs is related to the fabrication process using photoresist. By introducing cleaning process before the passivation, the reproducibility of the passivation was drastically improved. Long-term stability of the passivation was secured by a SiO_2 cover layer on the PMMA passivation film.

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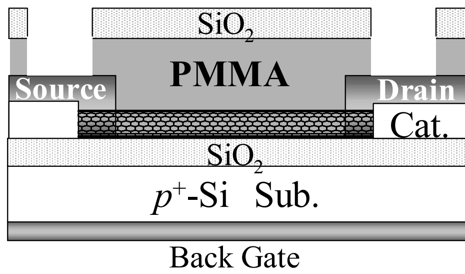


Fig.1 Schematic structure of carbon nanotube FETs.

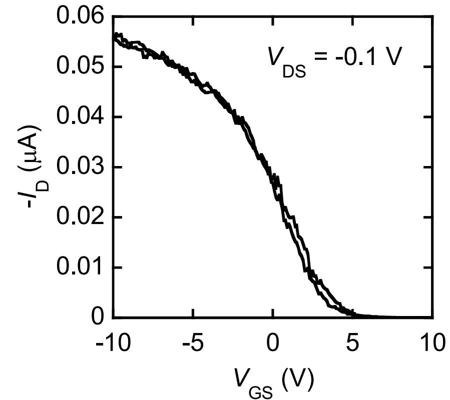
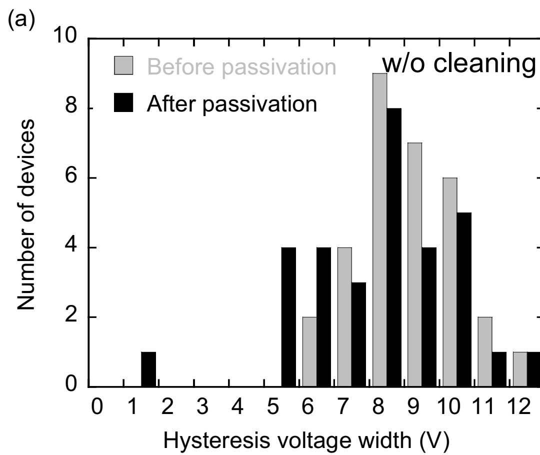


Fig. 2 I_D-V_{GS} characteristics of SiO_2/PMMA-passivated device.



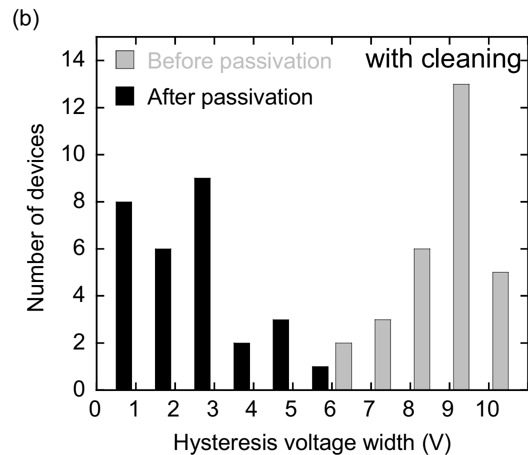
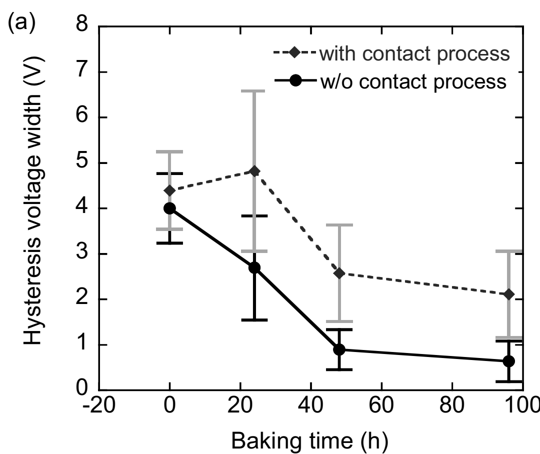


Fig. 3 Histogram of the hysteresis voltage width of the devices with SiO_2/PMMA passivation; (a) without cleaning process, and (b) with cleaning process.



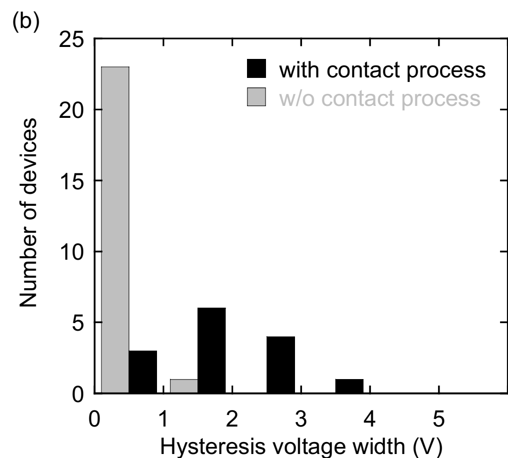


Fig. 4 Effect of process to form contact electrodes. (a) Variation of hysteresis by baking in vacuum for batches with and without process. (b) Comparision of hysteresis voltage width between two batches with and without process after baking for 96 h.